TE-SEM VI (R-2012) - EXTC (CBSGS)

Dec 2015

QP Code : 6491

VLSI Design.

(3 Hours) **[Total Marks : 80**

N.B.: (1) **Question No. 1** is compulsory. Solve any **three** from the remaining **five** questions.
(2) Figures to right indicate full marks.
(3) Assume suitable data if required and mention the same in the answer sheet.

1. Solve **any five** from the following **20**
   a) Explain Level 1 and Level 2 MOSFET model used in circuit simulator.
   b) In 2 input CMOS NAND gate all PMOS transistors have $\left(\frac{W}{L}\right)_p = 20$ and all NMOS transistors have $\left(\frac{W}{L}\right)_n = 10$. Draw its equivalent CMOS inverter and find size of PMOS and NMOS transistor in the equivalent inverter circuit.
   c) What are advantages & disadvantages of dynamic logic circuit.
   d) Why sense amplifier is used in memory circuit. Explain its working.
   e) How low power circuit is designed through voltage scaling.
   f) Explain hot carrier effect in short channel MOSFET.

2. a) Compare resistive load inverter, saturated load inverter and CMOS inverter on the basis of Noise margins, power dissipation, area and delay. **10**
   b) Draw 2 input CMOS NOR gate and using equivalent inverter approach and derive expression for V_{IL}, V_{IH}, V_{OL} and V_{OH}. **10**

3. a) Design clocked D-FF and implement using standard CMOS logic style. **10**
   b) Draw layout of six transistor CMOS SRAM using lambda rule. **10**

4. a) Explain 4-bit x 4-bit array multiplier with the help of necessary hardware for the generation and addition of partial product. **10**
   b) Why ESD protection is required for CMOS chips. Explain various techniques of ESD protection. **10**

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5. a) Implement $y = \overline{A(D+E)+BC}$ using **10**
   i) Static CMOS style
   ii) Pseudo NMOS logic style
   iii) Dynamic logic style
   iv) Transmission Gate logic

   b) What are different types of MOSFET scaling? Explain advantages and disadvantages of each using appropriate equations. **10**

6. Write short notes on **any four** **20**
   i) 3T-DRAM cell
   ii) Clock distribution in VLSI system
   iii) Barrel shifter
   iv) C^2MOS logic style
   v) 1-bit shift register
